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2008 Jpn. J. Appl. Phys. 47 6236

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Thermal Analysis of Degradation in Ga$_2$O$_3$–In$_2$O$_3$–ZnO Thin-Film Transistors

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(Received March 5, 2008; accepted April 14, 2008; published online August 8, 2008)

Degradation of Ga$_2$O$_3$–In$_2$O$_3$–ZnO (GIZO) thin-film transistors (TFTs), which are promising for driving circuits of next-generation displays, was studied. We found a degradation mode that was not observed in silicon TFTs. A parallel shift without any change of the transfer curve was observed under gate voltage stress. Judging from the bias voltage dependences we confirmed that the mode was mainly dominated by a vertical electric field. Thermal distribution was measured to analysis the any change of the transfer curve was observed under gate voltage stress. Judging from the bias voltage dependences we concluded that Joule heating did not accelerate degradation. Recovery of electrical properties independent of stress voltage were observed. [DOI: 10.1143/JJAP.47.6236]

KEYWORDS: thin film transistor, Ga$_2$O$_3$–In$_2$O$_3$–ZnO, reliability, degradation, threshold voltage stress, recovery

1. Introduction

In recent years, oxide semiconductors$^{1-4}$ have attracted considerable attention as promising materials for the driving thin-film transistors (TFTs) of new displays such as organic light-emitting displays. Positive features of this material, as compared with amorphous silicon TFTs, are low fabrication temperature lower than 200°C and considerably high electrical properties, such as mobility, and low threshold voltage. Such a high performance enables us to design a peripheral circuit. Furthermore, owing to their wide band gap, they are regarded as suitable materials for “transparent electronics”.$^{1,2}$

On the other hand, several papers$^{5-7}$ have reported the poor stability of oxide semiconductors against electric stress. Therefore, reliability is one of the serious problems for the realization of a new display using oxide semiconductors. However, no studies have analyzed the degradation systematically. In particular, there are few reports on TFT degradation under circuit operation.$^{8,9}$

In this study, we evaluated the reliability of oxide semiconductor TFTs with amorphous Ga$_2$O$_3$–In$_2$O$_3$–ZnO (GIZO)$^{10}$ by applying gate and drain voltage stress. We discussed the degradation caused by drain voltage and/or current flow assuming circuit operation. A thermal imaging system$^{10}$ was used to analyze thermal distribution during the stress and we discuss in this paper the degradation mechanism.

2. Experimental Procedure

A schematic cross-sectional image of a GIZO TFT$^{10}$ is shown in Fig. 1. On a glass substrate, Mo metal was deposited by sputtering. After the patterning of the gate metal by wet etching, a SiN film with a thickness of 400 nm was deposited by definition Plasma Enhanced chemical vapor deposition (PECVD) at 300°C as a gate insulator. Then a GIZO film with a thickness of 70 nm was deposited in a mixture of Ar and oxygen gases. After patterning of the active layer, the source and drain electrodes were formed by the lift-off process. A GIZO source/drain was fabricated by rf sputtering. Finally, the fabricated TFT was annealed for 1 h at 350°C in N$_2$ ambient.

The gate sizes of the TFTs used in this study ranged from 10 to 20 μm in length and 60 to 180 μm in width. For these TFTs, various gate and drain voltages were applied as electric stress and changes in electrical properties were examined to evaluate reliability. To analyze the degradation mechanism, thermal analysis using a thermal imaging system (Infra Scope II) was performed.

In order to measure the recovery of electrical properties, changes of the transfer curves were examined immediately after removing the stress.

3. Results and Discussion

3.1 Initial electrical properties

Figure 2(a) shows the electrical properties of the GIZO TFT measured at a drain voltage of 5.0 V. A good transfer curve indicates a steep slope at about $V_g = 0$ V, and an ON/OFF ratio higher than 8 digits. A high mobility over 2.6 cm$^2$/V-s and a very low leakage current were obtained. Figure 2(b) shows an excellent output curve without any kink current. A steep rise in the low drain region suggests a good ohmic contact.

3.2 Threshold voltage shift caused by gate voltage

Figures 3(a) and 3(b) show changes in transfer characteristics and field effect mobility caused by a gate voltage stress of 20 V. With time, the transfer curve and peak mobility shifted parallel to the positive direction. Marked changes in the $S$ parameter and mobility were not observed. A parallel shift without mobility change suggests the generation of electron traps without causing interface state generation.
3.3 Bias voltage dependence of threshold voltage stress

Threshold voltage shift under various bias voltage stresses is shown in Fig. 4. The threshold voltage shift showed a logarithmic change with stress time in the gate voltage range. The amount of shift increased with voltage. The slopes of the curves were approximately from 0.2 to 0.4. The slope decreased with increasing gate voltage stress. These values indicated the electron trap at the interface. Therefore, we suppose that electron trapping was accelerated by the increase in gate electric field.

3.4 Gate size dependence of threshold voltage shift

As shown in Fig. 5(a), threshold voltage shift under a gate voltage stress of 20 V was measured for TFTs with various gate widths. The gate widths varied from 60 to 150 μm. The amount of shift exhibited a logarithmic change with stress time for all TFTs. The amount of shift depended on gate size. Their slopes approximately 0.4 were independent of gate size.

Furthermore, gate length dependence was measured for a gate voltage stress of 30 V as shown in Fig. 5(b). The gate lengths varied from 5 to 20 μm. With the increase in gate length, the amount of the shift increased. However, all TFTs showed constant slopes. These slopes were similar to those obtained in Fig. 5(a).

Drain current does not flow under gate voltage stress. Therefore, these dependences suggest that the threshold voltage shift is dependent on gate area. With increasing gate area, the probability of trap generation increases, consequently, degradation is enhanced.

3.5 Recovery

Figure 6(a) shows the recovery of electrical properties after stress imposition. After the imposition of a gate voltage stress of 20 V, recovered electrical properties were measured without any stress at room temperature. Immediately after turning off the stress, the transfer curves recovered gradually with time. Recovery of threshold voltage shifts were plotted with time in Fig. 6(b). Independent of stress bias, they showed logarithmic changes against time.

Drain current does not flow under gate voltage stress. Therefore, these dependences suggest that the threshold voltage shift is dependent on gate area. With increasing gate area, the probability of trap generation increases, consequently, degradation is enhanced.
3.6 Degradation by drain voltage stress

As described above, we measured the degradation caused by only the gate voltage stress. Here, we investigated the effects of drain bias. To study the degradation of the TFTs under operation in the peripheral circuits, the effects of the drain bias are very important. Figure 7(a) shows the changes of the transfer curves under the stress of gate and drain voltage, \( V_g = V_d = 20 \text{ V} \). The shift of the transfer curve was similar to that in the case of gate-only stress shown in Fig. 3, that is, a parallel shift was observed with time. This similar change suggests that the degradation mode was not changed by the addition of drain voltage stress. Figure 7(b) shows the threshold voltage shift under various drain voltage stresses at a fixed gate voltage of 20 V. With increasing drain voltage, a marked increase in the amount of shift was not observed even at \( V_d = 30 \text{ V} \). Slopes were almost the same and close to those obtained using gate-only stress.

The effect of gate size was also examined under drain voltage stress \( (V_g = V_d = 20 \text{ V}) \) as shown in Fig. 8, using TFTs with various gate widths. The amount of shift depended on the width. However, compared with the gate-only stress shown in Fig. 5(a), the effect of drain bias on size dependence was very small. Therefore, even under drain current flowing conditions, the effect of gate size was not confirmed.

Recovery of electrical properties were also measured under a drain voltage stress of \( V_g = V_d = 20 \text{ V} \), as shown in Fig. 9. Even for this stress, recovery of the transfer curve was observed, that is, it recovered to almost the initial level. The shift of threshold voltage was plotted against time, as shown in Fig. 9(b). The slope of the recovery was independent of stress voltage, and was close to the value observed under gate-only stress shown in Fig. 6(b). These similarities also suggest that the degradation mode does not change with the addition of drain voltage shift. Therefore, immunity of the TFTs used in this study is high against drain voltage or drain current.

The imposition of drain voltage stress gave us concern regarding the damage caused by Joule heat. We previously reported that the Joule heat arising from drain current causes serious problems in the reliability of silicon TFTs. Hence, we investigated the thermal distribution of TFTs.

3.7 Analysis of thermal distribution

Figure 10 shows the thermal images obtained using a thermal infrared imaging system (Infra Scope II). These
images show the thermal distribution of TFTs under various drain voltages at a fixed gate voltage of 20 V. This is the first report on the thermal images of oxide semiconductor TFTs. For a drain bias of 0 V, no thermal distribution was observed. With increasing drain voltage, temperature increased. For a drain voltage of 20 V, temperature increased to around 90°C. Careful observation revealed that the position of maximum temperature was somewhat close to the drain region. These drain voltage dependences suggest that temperature increase is caused by Joule heating arising from drain current.

Thermal analysis of the TFTs with various gate widths was performed and results are shown in Fig. 11. A marked increase in the maximum temperature was observed with increasing gate width. In the TFT with a gate width of 200 μm, a maximum temperature of 130°C was observed. With an increase in gate width, heat dissipation will be insufficient. Therefore, the maximum temperature increased in wide gate TFTs.
From the results shown in Figs. 10 and 11, a marked increase in temperature caused by drain voltage and gate width was observed. However, we found that Joule heating does not accelerate the degradation observed in these TFTs.

3.8 Degradation mechanism

In this study, a peculiar degradation mode was observed in the GIZO TFTs. The main feature of this degradation is a parallel shift without any change in the transfer curve was observed. Judging from the bias voltage dependence, we confirmed that the mode was mainly dominated by a vertical electric field. A marked acceleration of degradation caused by drain bias stress was not found. Thermal analysis was performed to investigate the degradation mechanism. Temperature increases caused by drain voltage or gate size change were observed, however, Joule heating did not accelerate the degradation. Recovery of electrical properties independent of the stress bias condition were observed.

Acknowledgements

The authors thank Professor M. Kimura of Ryukoku University and Professor T. Kamiya of Tokyo University of Technology and Professor M. Furuta of Kochi University of Technology for fruitful advice.